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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/029,848	12/31/2001	Jae Hyung Lee	049128-5034	5336

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EXAMINER	
NELSON, ALECIA DIANE	
ART UNIT	**PAPER NUMBER**
2675	

DATE MAILED: 12/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/029,848	LEE ET AL.	
	Examiner	Art Unit	
	Alecia D. Nelson	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 11-14-05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. ***Claims 1-7, 11, 12, and 16-19*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimura (U.S. Patent No. 2001/0002829) in view of Youn (U.S. Patent No. 5,856,816).

With reference to **claims 1, 11, and 16**, Nishimura teaches a liquid crystal polarity inversion driver determining whether a polarity of a liquid crystal is inverted and inverting the polarity of the liquid crystal in accordance with the determined result (see paragraph 43-44); a first data polarity inversion driver (10-1) determining whether a first

data transition is occurred in the first data, and inverting the polarity of the first data in accordance with the determined result (see paragraph 49); a second data polarity inversion driver (10-2) determining whether a second data transition is occurred and inverting the polarity of the second data in accordance with the determined result (see paragraph 49).

While teaching dividing all data signals into groups which are feed to the data polarity inversion circuits (A-D), there is no disclosure towards the first set of data being odd data and the second set of data being even data.

Youn teaches first and second data polarity inversion of odd and even data in teaching a liquid crystal display wherein data is divided into even and odd portions externally from the drive IC and are fed through latch devices (22, 23), and are further latched in line latches storing odd (25) and even (26) line data. The line data of the line latches selects a corresponding voltage based on a signal from the line conversion logic (24).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow that the data be divided into even and odd groups as taught by Youn, to be used in a system similar to that which is taught by Nishimura, which allows for 2-port data polarity inversion. By allow such a combination a large high-resolution liquid crystal display with a reduction in frequency EMI and power consumption (see Youn column 1, lines 21-33; column 5, lines 44-53).

With reference to **claims 2, 3, 12, and 17**, Nishimura teaches that the first data polarity inversion driver includes, a first data transition part (11) determining whether the first data transition has occurred in the first/odd data and outputting a first signal (inv1) (see paragraph 53); a first data polarity inversion signal summer (12) counting the number of first signal that a data polarity is changed according to the first data transition and determining whether an output level is high or low (see paragraph 53); and a first data polarity inversion signal output part (15) receiving the first signal and the determined output level from the first data transition part and the first data polarity inversion signal summer and outputting an inverting signal (dd1-24) for inverting output data (paragraph 53, Fig. 4). With further reference to **claims 3 and 17**, Nishimura teaches that the components of data polarity inversion judgment units (10-1 through 10-4) have the same construction, therefore the construction of the second/even data polarity inversion driver (10-2) has the same construction to that which is described with reference to the first data polarity inversion driver (10-1) (see paragraph 52).

With reference to **claims 4, 5, and 18**, Nishimura teaches that the first and second data transition part includes first (13) and second (14) flip-flops and an exclusive logical sum gate (23) comparing current data with previous data to determine whether the first data transition has occurred in accordance with the compared result (see paragraph 53).

With reference to **claims 6, 7, and 19**, Nishimura teaches that the first and second data inversion signal summer includes an a first and second adder for adding the number of data with a data transition from the first and second data transition part; and a majority detector (22) determining whether the added number of the data is higher than a first reference value (see paragraph 53-57).

4. **Claims 8, 9, and 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimura in view of Youn as applied to **claims 1, 11, and 16** above, and further in view of Applicant's admittance of prior art.

Nishimura and Youn teach all that is required as explained above with reference to **claims 1, 11, and 16**, however fails to teach that the data polarity inversion signal output part includes a multiplexor receiving the signal from the summer to invert the output data. However, there is no disclosure of the usage of a summer and outputting inverted data as explained above.

Applicant's admitted prior art teaches as first data polarity inversion signal output part which includes a multiplexor (48, 50) receiving a first polarity inversion signal from the first data polarity inversion signal summer (32) to invert the output data (see paragraph 23).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow the output part to consist of a multiplexor, as disclosed by the applicant's admittance of prior art, in a system composed similar to that which is

taught by Nishimura and Youn as explained above to thereby provide a liquid crystal display which outputs inverted data to be applied to the liquid crystal panel in order to reduce the amount of change of data output which reduces power consumption and noise generated..

5. **Claims 14 and 15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimura in view of Youn as applied to **claims 1, 11, and 16** above, and further in view of Gooding et al. (U.S. Patent No. 4,580,265).

Nishimura and Youn teach all that is required as explained above with reference to **claims 1, 11, and 16** as explained above, however fail to teach that the total number of bits is 18 and the first and second data bits it 9 as recited in the claim.

Gooding et al. teaches an integrated circuit (10) connected to a second circuit (12) wherein the first circuit (10) receives the even and odd bytes of data to be transmitted to the second circuit (12), wherein the even and odd bytes of data each comprise nine binary bits. Thereby the total number of the input data bit is 18.

Therefore it would have been obvious to one having ordinary skill in the art to allow for the usage even and odd data bits being inputted into a IC as taught by Gooding, to be used in a system similar to that which is taught by Nishimura and Youn as explained above in order to reduce the transmission of erroneous data and thereby reduce the effects of EMI on the display (see Gooding et al. column 2, lines 13-26).

Response to Arguments

Applicant's arguments with respect to claims 1-9, 11-12, 14, and 15 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alecia D. Nelson whose telephone number is 571-272-7771. The examiner can normally be reached on Monday-Friday 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on 571-272-3638. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

7. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

adn/ADN
December 11, 2005

SUMATI LEFKOWITZ
SUPERVISORY PATENT EXAMINER